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1 **An efficient controller scheme for MPEG-2 video decoder**
Nam Ling; Nien-Tsu Wang; Duan-Juat Ho;
Consumer Electronics, IEEE Transactions on , Volume: 44 , Issue: 2 , May 19
Pages:451 - 458

[Abstract] [PDF Full-Text (620 KB)] **IEEE JNL**

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2 **MPEG-2 video decoder for DVD**
Nien-Tsu Wang; Chen-Wei Shih; Duan Juat Wong-Ho; Nam Ling;
VLSI, 1998. Proceedings of the 8th Great Lakes Symposium on , 19-21 Feb.
Pages:157 - 160

[Abstract] [PDF Full-Text (296 KB)] **IEEE CNF**

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3 **VLSI design of a bus arbitration module for the 68000 series of microprocessors**
Ososanya, E.T.; McGlone, M.D.; Strong, T.D.;
Southeastcon '94. 'Creative Technology Transfer - A Global Affair'., Proceedin the 1994 IEEE , 10-13 April 1994
Pages:398 - 402

[Abstract] [PDF Full-Text (444 KB)] **IEEE CNF**

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An efficient controller scheme for MPEG-2 video decoder

Nam Ling Nien-Tsu Wang Duan-Juat Ho
Center for Signal Process., Nanyang Technol. Inst. , Singapore;

This paper appears in: **Consumer Electronics, IEEE Transactions on**

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On page(s): 451 - 458
Volume: 44 , Issue: 2
ISSN: 0098-3063
Reference Cited: 4
CODEN: ITCEDA
Inspec Accession Number: 5942319

Abstract:
A video decoder with an efficient block-level-pipeline **controller** scheme for MPEG-2 MP@ML is presented. The architecture in most of the reported literature for MPEG-2 MP@ML video uses a 64-bit **bus** and a complex **bus arbitration** scheme to communicate with the external DRAM, the display, and the incoming FIFO. Our design imposes a certain order in the DRAM access by various processing units instead of allowing any processing unit within the decoder to **request bus** access **arbitrarily**. This efficient DRAM accessing order allows us to reduce **bus** width from 64 bits to 32 bits, without significantly increasing the embedded buffer sizes, and still meet the requirements for

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MPEG-2 MP@ML real-time decoding. The **bus arbitration** algorithm is also simple, allowing for a less complex **controller** design

Index Terms:

DRAM chips buffer storage code standards decoding digital signal processing chips system buses telecommunication standards video coding 32 bit DRAM FIFO MPEG-2 MP@ML real-time decoding MPEG-2 video decoder block-level-pipeline **controller** **bus arbitration** algorithm **bus** width **controller** design embedded buffer sizes processing units

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VLSI design of a bus arbitration module for the 68000 series of microprocessors

Ososanya, E.T. McGlone, M.D. Strong, T.D.
Dept. of Electr. Eng., Tennessee Technol. Univ., Cookeville, TN, USA;

This paper appears in: **Southeastcon '94. 'Creative Technology Transfer - A Global Affair'., Proceedings of the 1994 IEEE**

Meeting Date: 04/10/1994 - 04/13/1994
Publication Date: 10-13 April 1994
Location: Miami, FL USA
On page(s): 398 - 402
Reference Cited: 3
Inspec Accession Number: 4784033

Abstract:
Modern computer systems often are designed around a **bus** architecture. This, of course eliminates the need for complete point-to-point interconnection of all the devices attached to the **bus**. The major hurdle to this system is in resolving the conflicts that arise when more than one device wants to use the **bus** to communicate at a time. The job of resolving such conflicts is left to **bus arbitration** circuitry. A system designer using the MC68000 family is in some luck. This series of microprocessors has a limited set of lines built in to allow for external circuitry to **request** and receive the **bus** from the

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processor. However, having given up the **bus** the processor does nothing to decide who receives the **bus** next. This is left to external **arbitration** circuitry. This paper describes a VLSI chip designed to perform **bus arbitration** for the Motorola MC68000 series of microprocessors. With such a module, several devices (such as DMA, I/O **controllers**, and multiple microprocessors) can share a single **bus** while our device handles all **bus** conflicts using a priority scheme. The device is flexible, programmable, and compatible with the MC68000 family's **bus** architecture and their support chips

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Index Terms:

68000 series VLSI VLSI design **bus arbitration** circuitry **bus arbitration** module **bus** architecture conflict resolution microcomputers microprocessor chips microprocessors network synthesis point-to-point interconnection system buses 68000 series VLSI VLSI design **bus arbitration** circuitry **bus arbitration** module **bus** architecture conflict resolution microcomputers microprocessor chips microprocessors network synthesis point-to-point interconnection system buses

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